Section IV: Nonrecoverable SEU Effects

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Non-Recoverable SEE

Events which interrupt device function and do not recover without external interaction

These events may permanently damage the device

Three main types

- Latchup (SEL)
- Hard errors (SHE)
- Rupture/Burnout (SEGR/SEB)

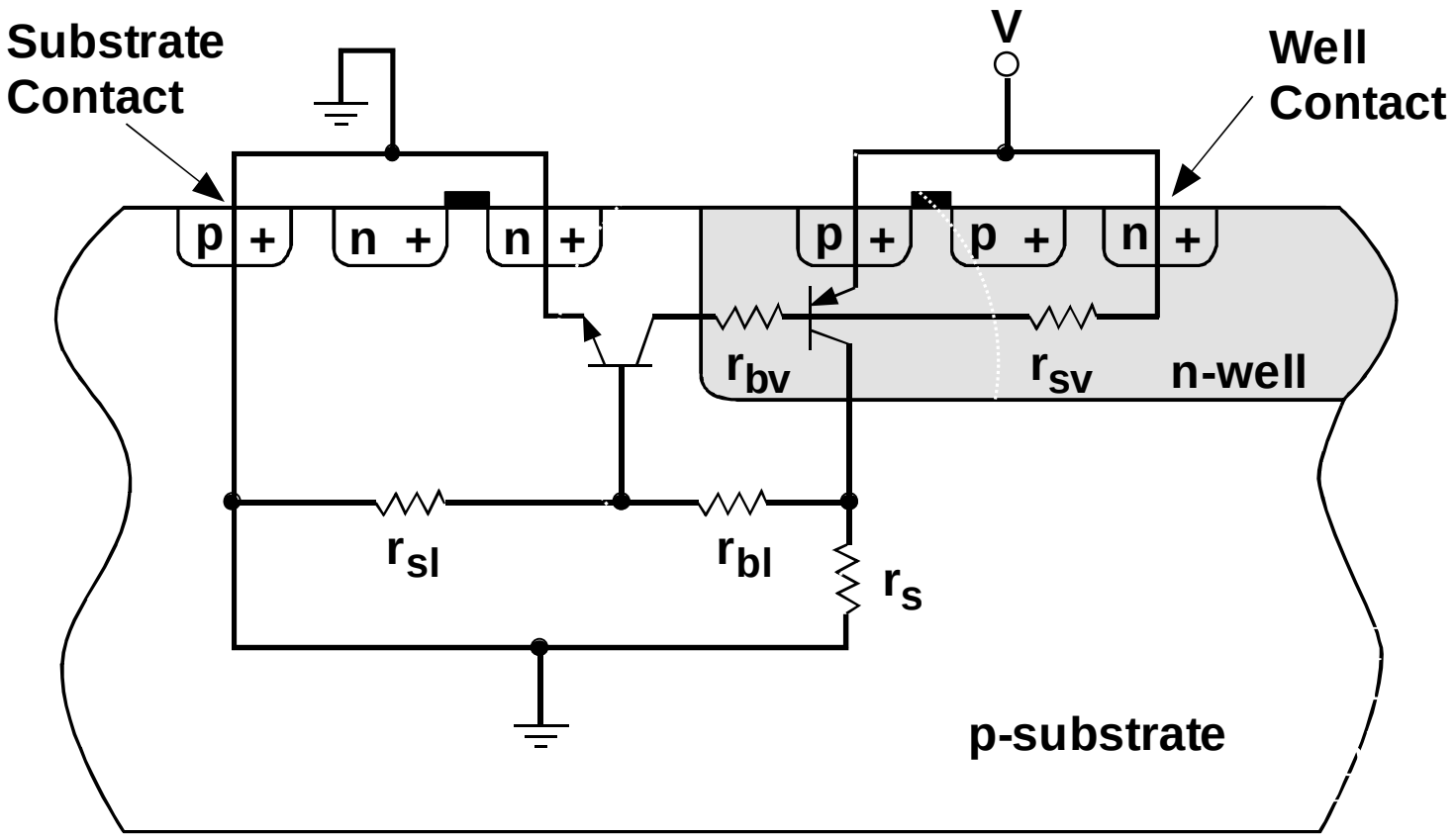
Latchup Is a Common Problem for CMOS Technology

Latchup paths are inherent in most CMOS circuits because of the fabrication technology

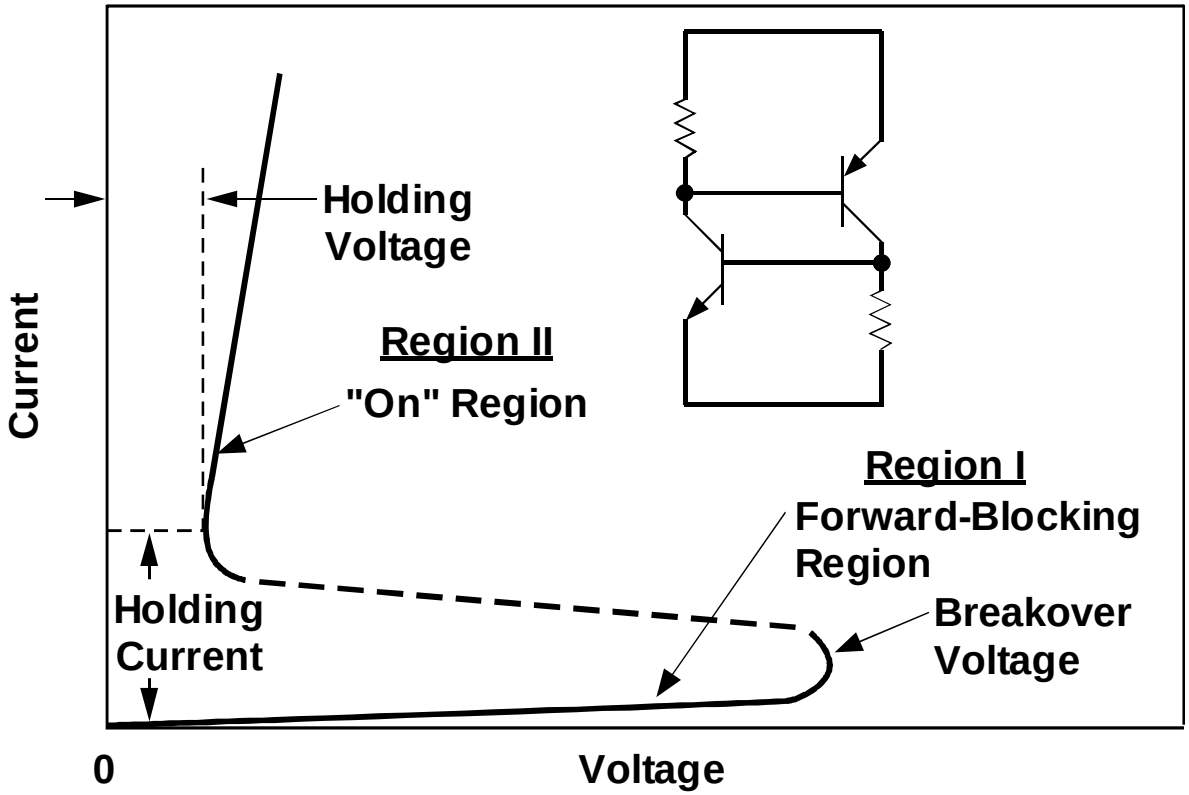
The commercial Modem on Pathfinder's Rover was susceptible to latchup

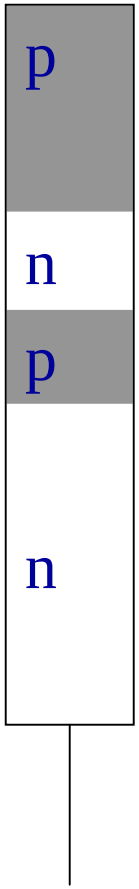
- Laboratory tests showed that the latchup was not destructive
  - This allowed the device to remain latched for periods of several minutes
  - A simple power cycle counter measure was used in the application
- The latchup probability was low for this application
  - Short mission life (nominally two weeks)
  - Risk deemed acceptable by mission planners

SEL Latchup Path



SEL I-V Characteristics





SEL Facts

Triggered by heavy ions, protons, neutrons

May be catastrophic

Only recovered by power cycle

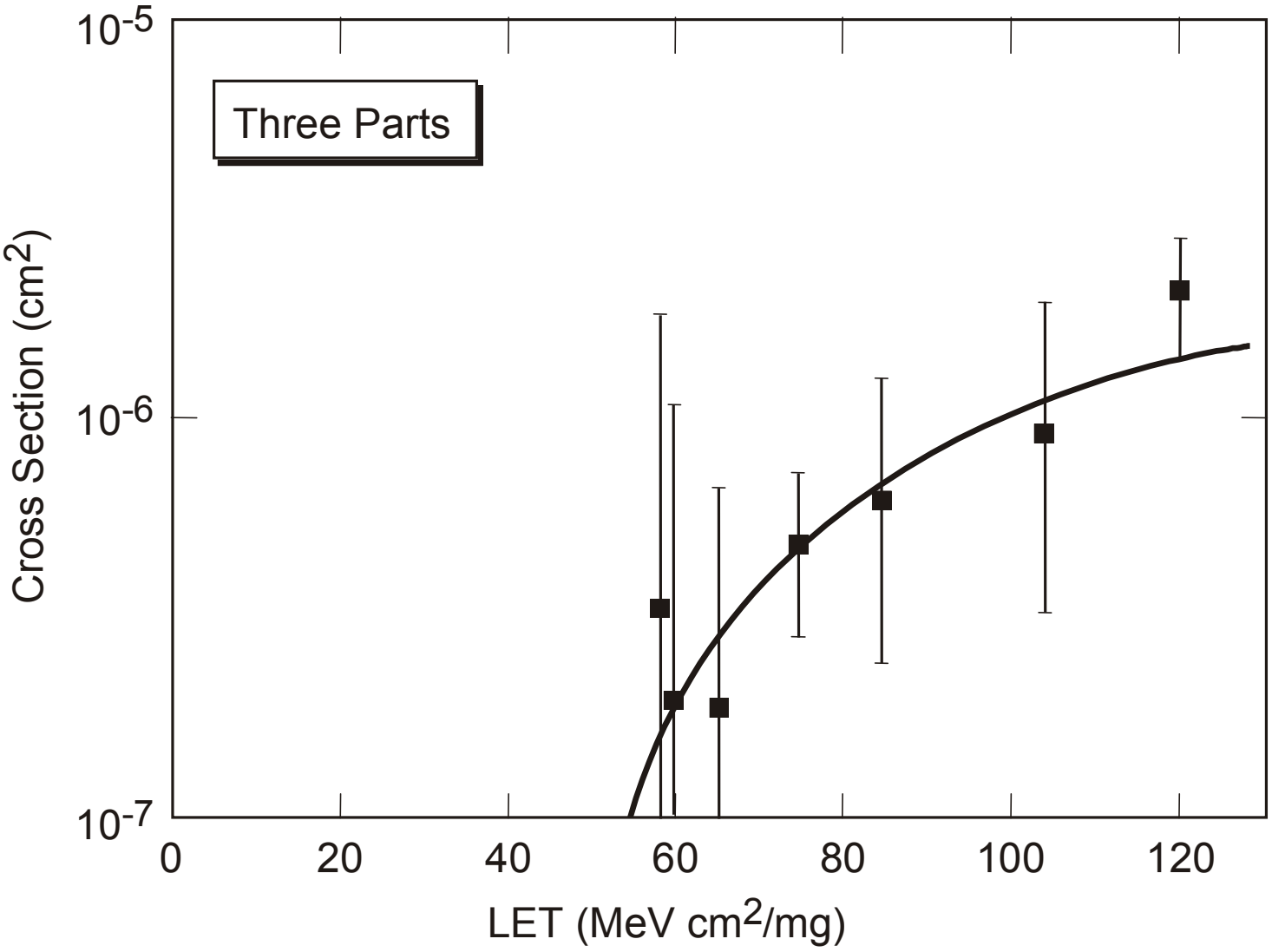
SEL is strongly temperature dependent

- Threshold for latchup decreases at high temperature
- Cross section increases as well

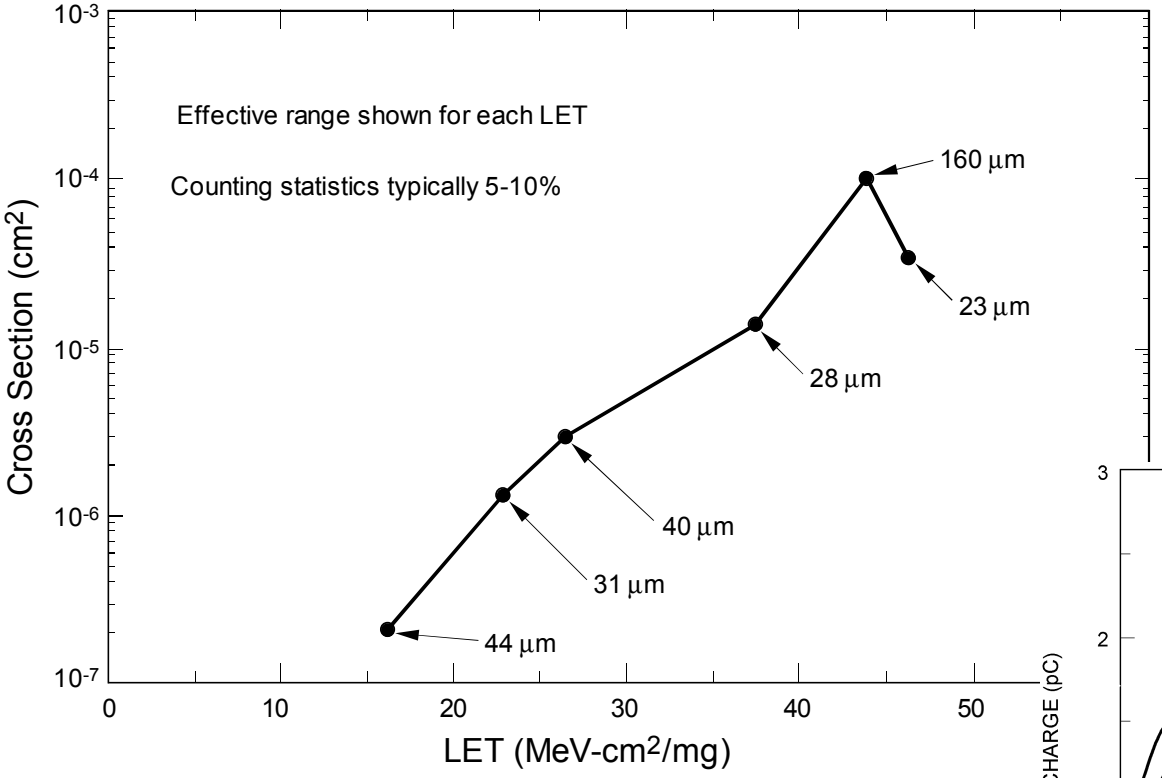
Modern devices may have many different latchup paths

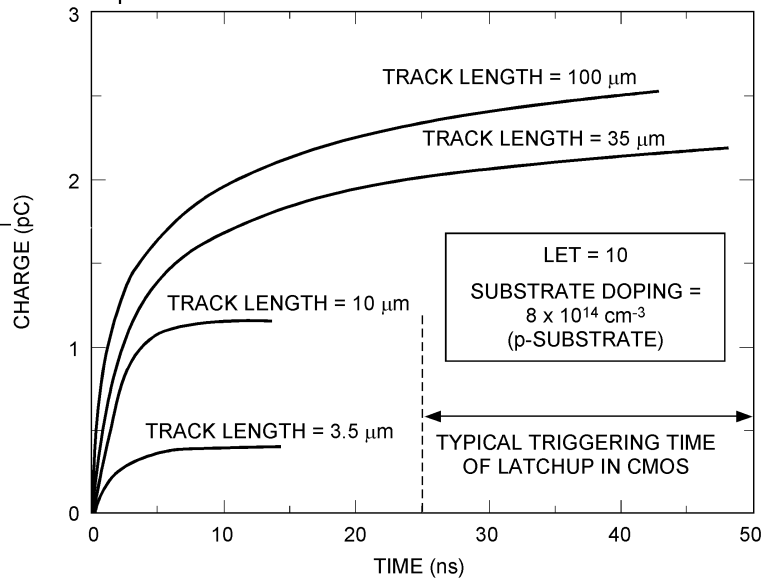
- Both high current and low current SELs can occur
- Characterization of latchup is a difficult problem for complex circuits

SEL LET Dependence

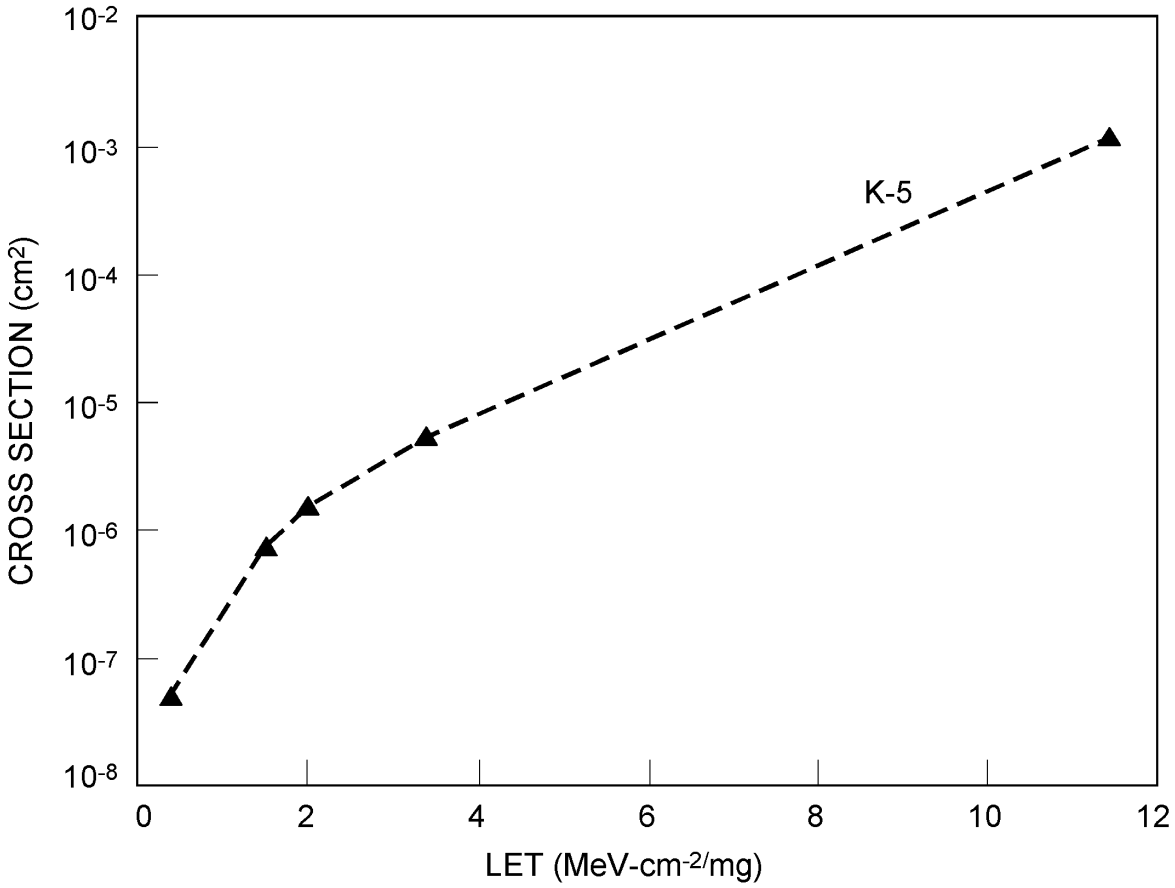


SEL Ion Range Dependence





SEL Example: Induced by Protons in K-5

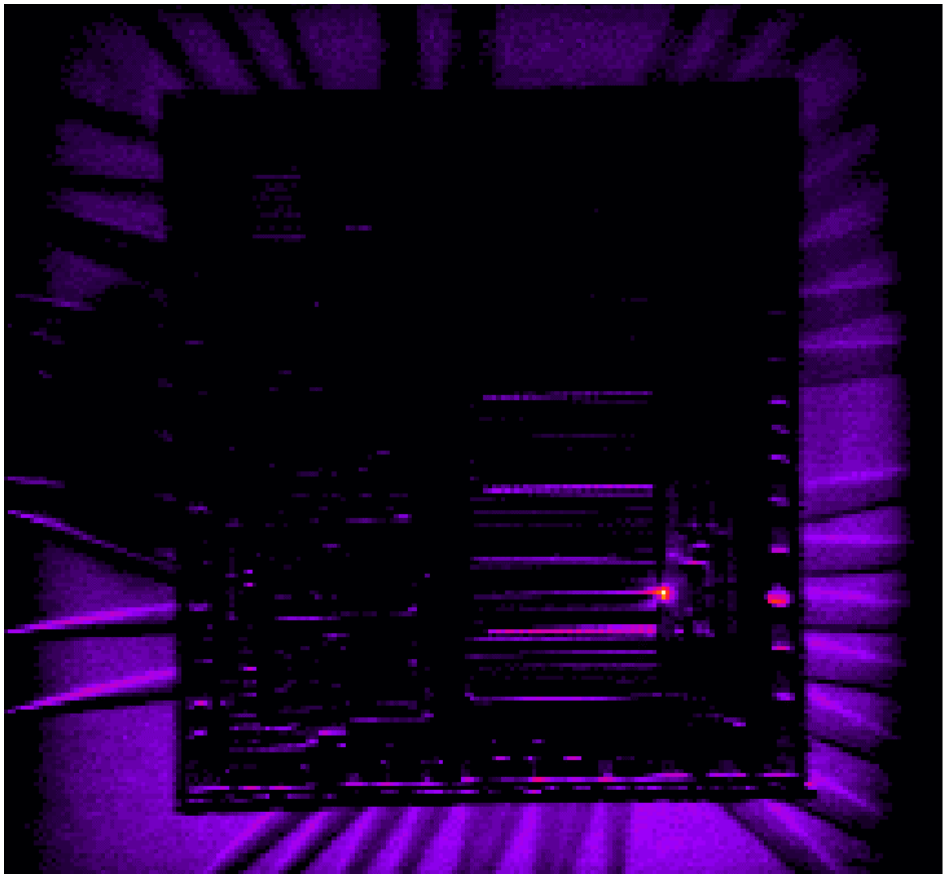


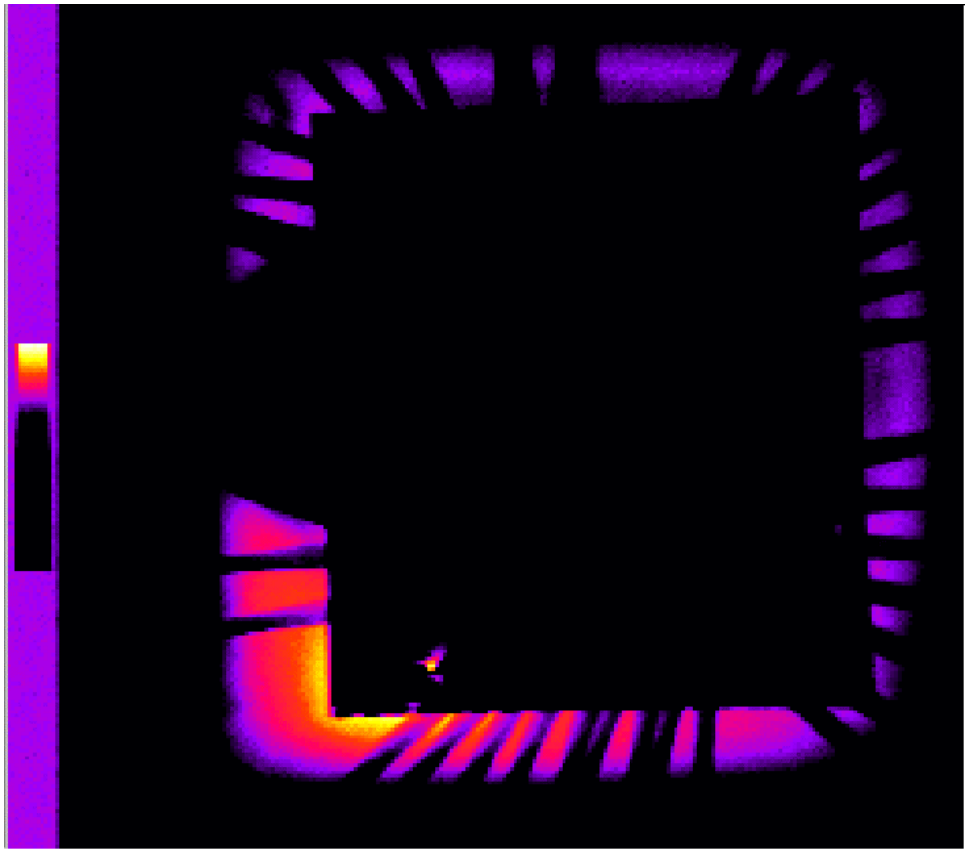
SEL occurred at 0.4 MeV cm²/mg

- **Due to nuclear recoils**
- **Cross section of 6.7×10^{-8} cm²**

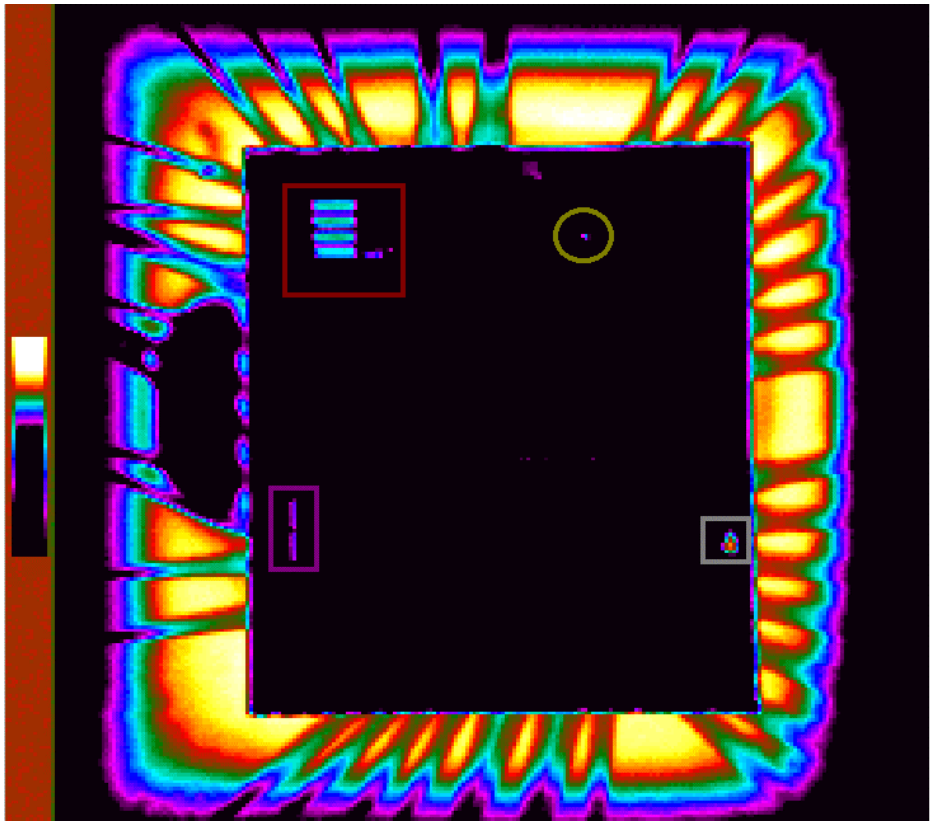
Many of the latchup events were destructive

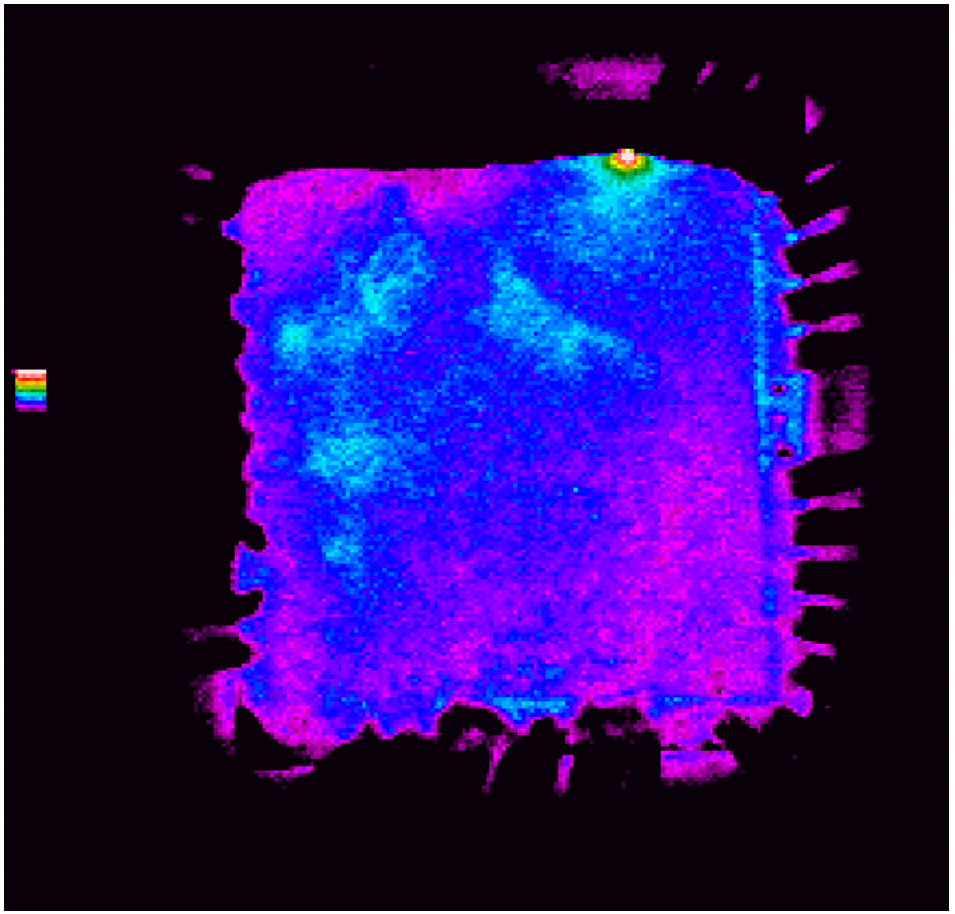
SEL Heating



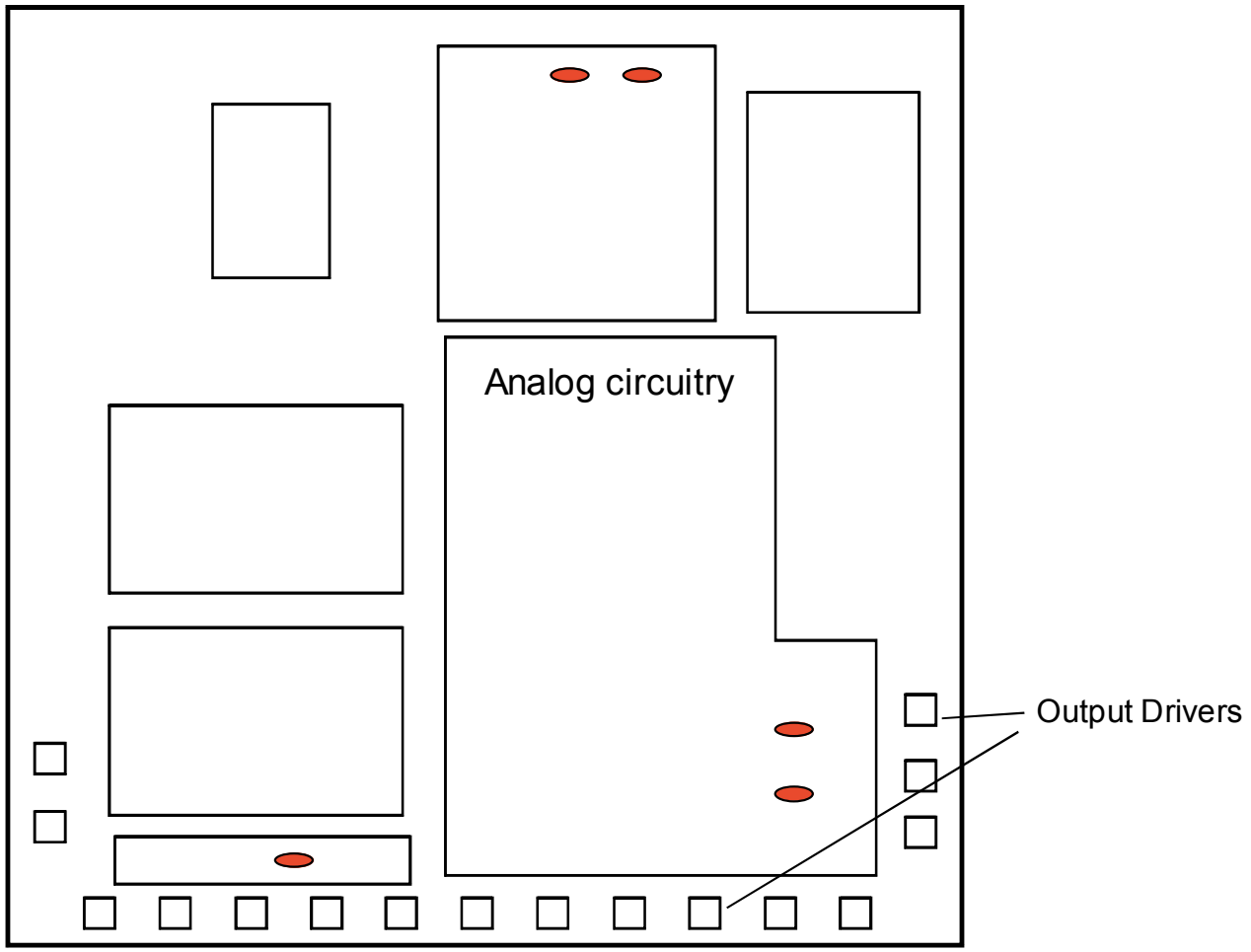


SEL Heating*

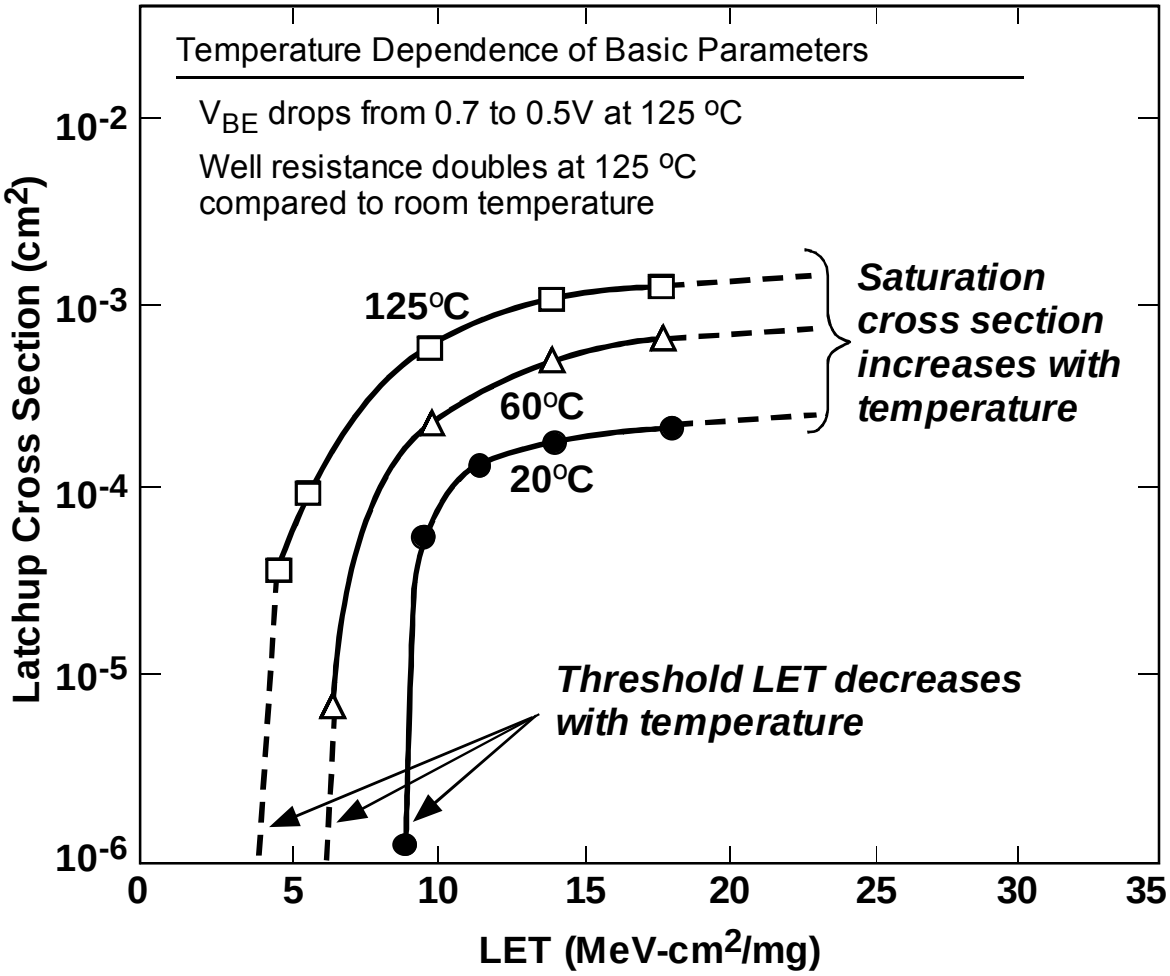




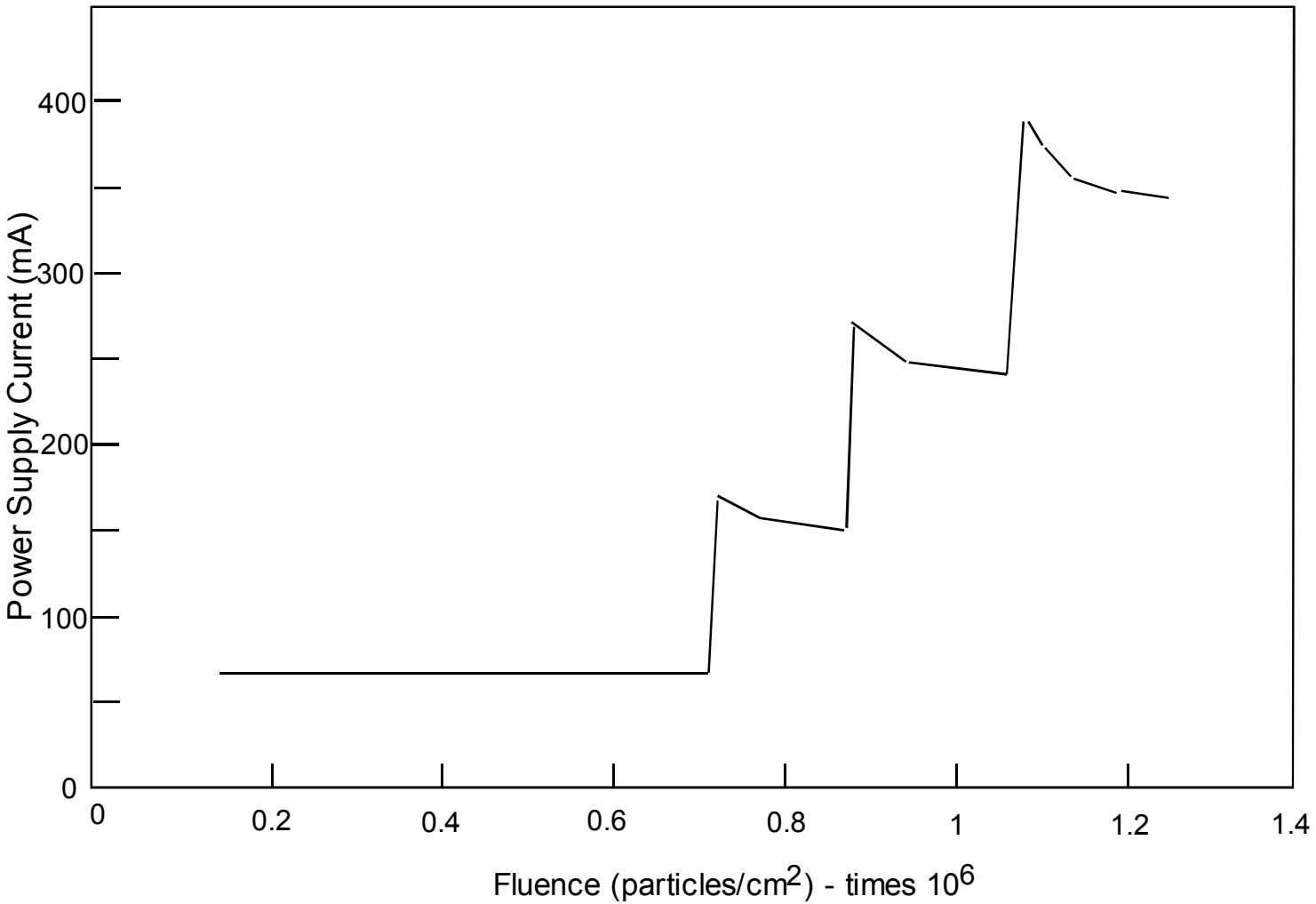
SEL Heating



SEL Temperature Dependence



SEL Temperature Dependence*



SEL Counter Measures

SEL Detection and Mitigation

- Current limiting devices can't stop latchups or low current latchups
- Detection circuits can't stop all latchups
  - Some devices have latchup modes which are always destructive
- Mitigation may not be fast enough
- Thorough testing required to ensure that all latchup events are detected

SEL Technology Options

Device type

- Bulk CMOS latches worst
  - **COTS**
- CMOS deposited on epitaxial layer may improve SEL immunity
  - **Some COTS - More Expensive**
  - **Not always effective (e.g., K-5 processor)**
- SOI and isolated oxides are mostly immune
  - **Very expensive**
  - **Limited availability**

Single Hard Errors

Large rare energy depositions can cause individual cells to be unable to change state

- Referred to as a “stuck bit” in memory
  - This is a microdose effect
- Microlatchups can cause a fraction of bits to be unable to change state
  - Power cycling is required

Destructive SEEs

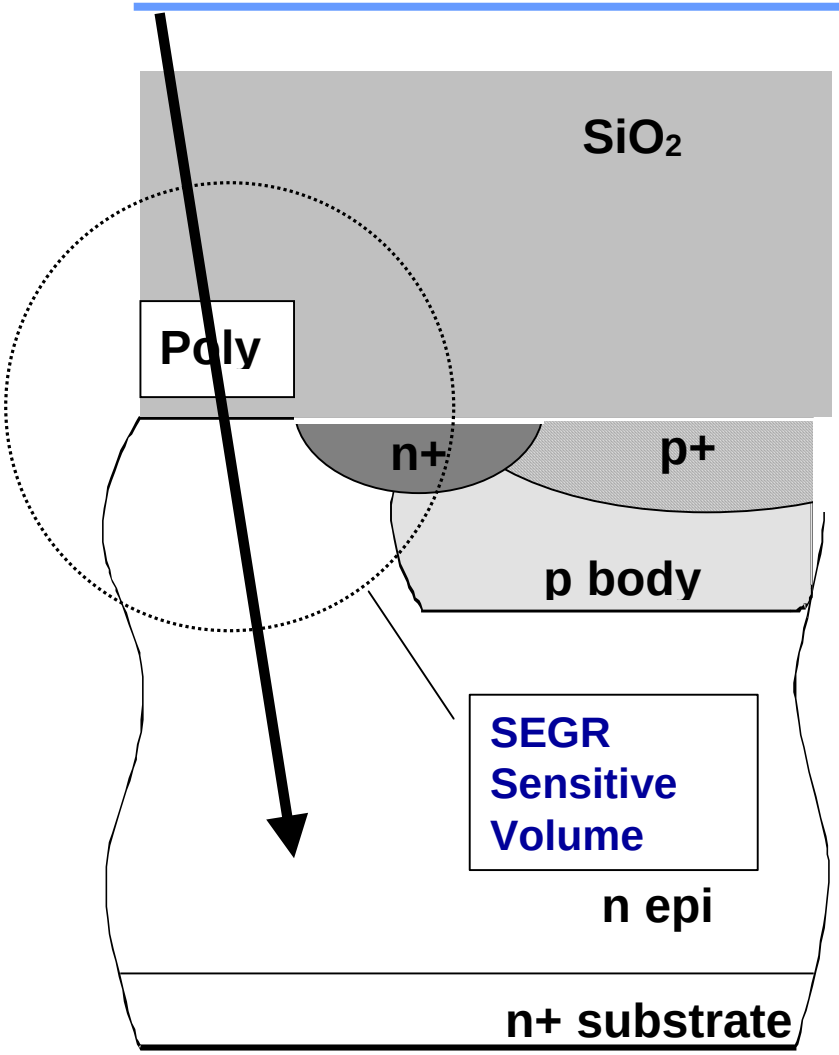
Gate Rupture (permanent failure of oxide)

- Power devices are most susceptible
- Programmable devices also susceptible
- Very thin oxides in VLSI devices

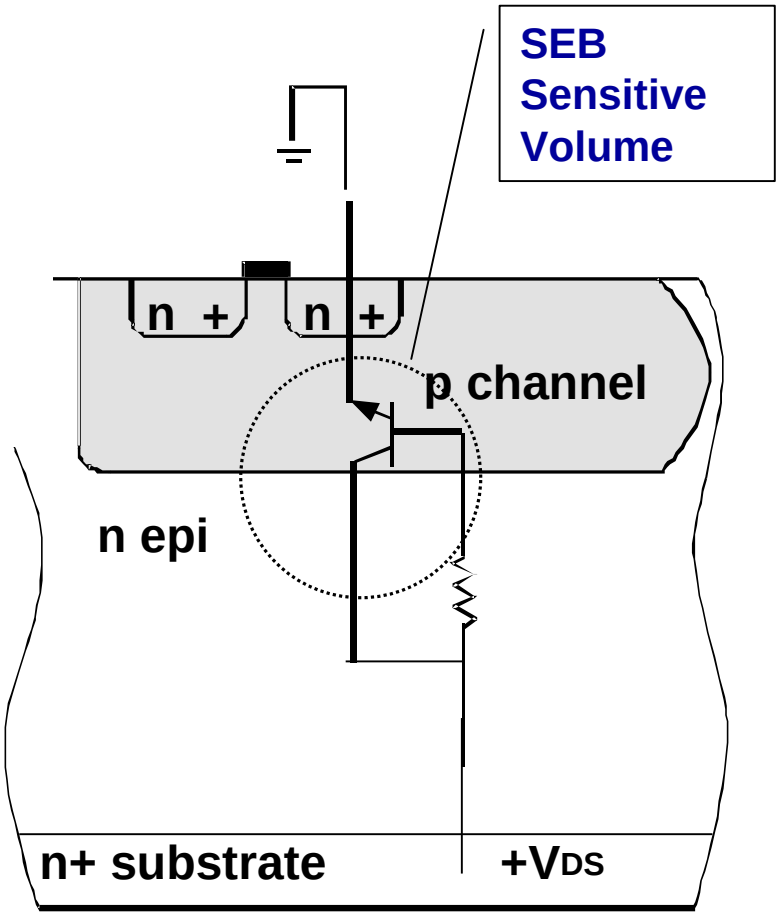
Burnout

- Caused by excessive localized current within the structure
- Power transistors
- Some types of linear integrated circuits

Destructive SEEs



Single Event Gate Rupture Power MOSFET



Single Event Burnout HEXFET

SEB Facts

Triggered by heavy ions, and possibly by protons and neutrons

Always destructive

CMOS, power BJTs and MOSFETs are susceptible

Mechanism:

- Localized current in body of device
- Roughly analogous to second breakdown in power transistors
- Devices with low doping concentrations are most susceptible

SEGR Facts

Triggered by heavy ions

Always destructive to device

Dependent on angle of incidence

Dependent on electric field in gate oxide

- **May also occur with zero electric field**
- **Interplay between pulsed current in drain region and oxide field**

Synergy between TID and SEE

Power MOSFETs most susceptible

- **Some modern programmable devices are also susceptible**

SEGR/SEB Examples

SEGR

EEPROM
- During writing/erasing

LAMBDA ASIC

Power MOSFET
- LET threshold of 25 MeV-cm^2/mg with drain biased at 1/2 rated maximum, and zero voltage on gate

SEB

CRUX/APEX
- 2N6796 had a LET threshold of 15 MeV-cm^2/mg

Dealing with SEGR and SEB

Test all device types that are potentially susceptible

Derate devices well below maximum rated values

- Possible for discrete power devices
- Not appropriate for SEGR or SEB in integrated circuits

Minimize duty cycle for application of high voltage to susceptible parts

Program high voltage device in low radiation environments

Summary

Latchup

- Temperature dependent
- Epi devices are generally better
- Prevention circuits not necessarily effective
- Best approach is to avoid using latchup-prone devices

Gate Rupture and Burnout

- High voltage devices are generally more susceptible
- Derate devices well below maximum operating conditions
- Ensure that all sensitive technologies undergo testing